(claims 1-21 Cert. Amd.

What is claimed is:

Sub B2 1. A printed circuit board formed by laminating an interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer, characterized in that the conductor circuit is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer is formed on at least a part of the surface of the conductor circuit.

2. A printed circuit board formed by laminating an interlaminar insulating layer on a conductor circuit of a substrate and repeating formation of conductor circuit and an interlaminar insulating layer, characterized in that the conductor circuit is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer is formed on at least a part of the surface of the conductor circuit, and the surface of the roughened layer is covered with a layer of a metal having an ionization tendency of more than copper but less than titanium or a noble metal.

3. A printed circuit board according to claim 1 ~~or 2~~, wherein the roughened layer is formed on at least a part of the ~~surface inclusive of a side surface of the conductor circuit~~.

Sub B1 A 4. A printed circuit board according to claim 1 ~~or 2~~, wherein the roughened layer is formed on at least a part of the side face of the conductor circuit.

A A 5. A printed circuit board according to ~~anyone of claims 1-4~~ claim 1, wherein the roughened layer is a plated layer of copper-nickel-phosphorus alloy.

Sub B4 ~~6. A method of producing a multilayer printed circuit board comprising steps of subjecting a surface of a substrate to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing~~

the plating resist, etching and removing the electroless plated film beneath the plating resist to form a conductor circuit comprised of the electroless plated film and the electrolytic plated film, forming a roughened layer on at least a part of the surface of the conductor circuit and then forming an interlaminar insulating layer.

7. A method of producing a multilayer printed circuit board comprising steps of subjecting a surface of a substrate to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form a conductor circuit comprised of the electroless plated film and the electrolytic plated film, forming a roughened layer on at least a part of the surface of the conductor circuit, covering the surface of the roughened layer with a layer of a metal having an ionization tendency of more than copper but less than titanium or a noble metal and forming an interlaminar insulating layer.

8. A method of producing a printed circuit board according to claim 6 ~~or 7~~, wherein the roughened layer is formed by plating of copper-nickel-phosphorus alloy.

Sub C85 9. (Amended) A multilayer printed circuit board comprising a substrate provided with an under layer conductor circuit, an interlaminar insulating layer formed thereon and an upper layer conductor circuit formed on the interlaminar insulating layer, and a viahole connecting both the conductor circuits to each other, in which the viahole is comprised of an electroless plated film and an electrolytic plated film, and a roughened layer having a roughened surface formed by etching treatment, polishing treatment, or redox treatment, or having a roughened surface formed by a plated film is formed on at least a part of the surface of the underlayer conductor circuit

connected to the viahole.

10. A multilayer printed circuit board according to claim 9, wherein the roughened layer is formed by plating of copper-nickel-phosphorus alloy.

11. (Amended) A method of producing a multilayer printed circuit board comprising steps of forming a lower conductor circuit layer on a surface of a substrate, forming a roughened layer by etching treatment, polishing treatment, redox treatment, or plating treatment on at least a part of the surface of the underlayer conductor circuit connected to a viahole, forming an interlaminar insulating layer thereon, forming openings for viaholes in the interlaminar insulating layer, subjecting the interlaminar insulating layer to an electroless plating, forming a plating resist thereon, subjecting the substrate to an electrolytic plating, removing the plating resist, etching and removing the electroless plated film beneath the plating resist to form an upperlayer conductor circuit comprised of the electroless plated film and the electrolytic plated film and a viahole.

12. A method of producing a multilayer printed circuit board according to claim 11, wherein the roughened layer is formed by plating of copper-nickel-phosphorus alloy.

13. A printed circuit board provided with a conductor layer used as an alignment mark, in which a roughened layer is formed on at least a part of the surface of the conductor layer.

14. A printed circuit board provided with a conductor layer used as an alignment mark, in which the conductor layer is comprised of an electroless plated film and an electrolytic plated film.

15. A printed circuit board according to claim 13 or 14, wherein the alignment mark is an opening portion formed by

exposing only the surface of the conductor layer from a solder resist formed on the conductor layer.

16. A printed circuit board according to ~~anyone of~~ claims 15, wherein a ~~metal layer~~ of nickel-gold is formed on ~~the conductor layer exposed from the opening portion~~.

17. A printed circuit board according to claim 13, wherein the conductor layer is comprised of an electroless plated film and an electrolytic plated film.

18. A printed circuit board according to claim 14, wherein the roughened layer is formed on at least a part of the surface of the conductor layer.

19. A printed circuit board according to anyone of ~~claims 13-18~~ claim 13, wherein the alignment mark is used for positioning to a printed mask.

20. A printed circuit board according to anyone of ~~claims 13-18~~ claim 13, wherein the alignment ~~mark is used for an IC chip~~ mounting.

21. A printed circuit board according to anyone of ~~claims 13-18~~ claim 13, wherein the alignment mark is used for positio ning in the mounting of a printed circuit board packaged a s emiconductor element to another printed circuit board.